REMARKS

This is a full and timely response to the outstanding Action mailed December 11, 2006. Upon entry of the amendments in this response, claims 1, 4-6, 10-14, 16, 18 and 20 remain pending. In particular, Applicant has amended independent claims 1, 5, and 11 and has canceled claims 15, 17, and 19 without waiver, disclaimer, or prejudice to the subject matter previously embodied therein. In this regard, claims 1, 5, and 11 further recite the limitation of "a portion of the pixel electrode is substantially located between the gate and the compensation structure and substantially spaced apart from at least one of the gate and the compensation structure". Support for these amendments can be found at various portions of the application. By way of example, Figs. 3A, 3B, 6, and 7 show that a portion of the pixel electrode 114 is disposed between the gate G and the compensation structure(s) 102a/102b. As the original application fully supports the subject matter of the claim amendments, the amendments add no new matter to the application. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Indication of Allowance Subject Matter

Applicant notes with appreciation the Examiner's indication that claims 15, 17 and 19 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Rejections under 35 U.S.C. 103

The Office Action indicates that claims 1, 4-5, 10-14, 16, 18 and 20 stand rejected under 35 U.S.C 103(a) as allegedly unpatentable over Ukita (US Pat. 6,310,668) in view of Moon (US Pat. 7,075,595) and claim 6 stands rejected under 35 U.S.C 103(a) as being unpatentable over Ukita and Moon in view of Fujikawa (US Pat. 5,995,178). Applicant respectfully traverses the rejections.

With respect to Ukita, Ukita discloses several embodiments (mainly indicated as prior art) relevant to a LCD device with compensation structure. In one embodiment, the device includes a gate electrode 32 and a compensating gate electrode 61 which are so arranged as to extend in a direction perpendicular to a longitudinal direction of a gate bus wiring 33. A compensating source electrode 62 is disposed over both the source electrode 40 and the compensating gate electrode 61 in a partially overlapping relationship therewith. Additionally, the protruded portion of the pixel electrode 42 has a left side and a right side. The left side of the protruded portion of the pixel electrode 42 overlaps the gate electrode 32 and the right side overlaps the compensating gate electrode 61 (See col. 4, lines 31-37, and Fig. 11). Applicant notes that the pixel electrode 42 disclosed by Ukita is not located between the gate electrode 32 and the compensating gate electrode 61 and spaced apart from the gate electrode 32 and the compensating gate electrode 61.

With respect to Moon, Moon discloses an array substrate for an LCD device, in which a source electrode 119 is extended from a data line 125 and has a "U"-shape. A rectangle-shaped opening is formed in a portion for a gate electrode 115 in the gate line 113. A drain electrode 117 is formed over the rectangle-shaped opening of the gate

electrode 115 and has an inverted "T"-shape. Only end sides of the drain electrode 117 overlap the gate electrode 115 (See col. 8, lines 40-49 and Fig. 8). Applicant notes that the drain electrode 117 connected to a pixel electrode 225 disclosed by Moon is not located between both sides of the rectangle-shaped opening formed in the gate electrode 115 and spaced apart from both sides of the rectangle-shaped opening formed in the gate electrode 115.

Turning now to the independent claims of the present application (as amended herein), claim 1 recites:

> 1. A liquid crystal display device with a capacitance-compensated structure, comprising:
> a gate line;
> a gate electrically connected to the gate line;
> a compensation structure extending from at least one of the gate and the gate line;
> a drain having a first side and a second side, wherein the first side of the drain overlaps a portion of the gate and the second side of the drain overlaps a portion of the compensation structure; and
> ***a pixel electrode disposed on a part of the drain and electrically connected to the drain through a via, so that a portion of the pixel electrode is substantially located between the gate and the compensation structure and substantially spaced apart from at least one of the gate and the compensation structure.***

(*Emphasis Added*).

Claim 5 recites:

> 5. A liquid crystal display device with a capacitance-compensated structure, having a gate line and a data line to turn a thin film transistor on or off, comprising:
> a gate electrically connected to the gate line;
> a drain having a first side and a second side, wherein a first parasitic capacitor is formed between the first side of the drain and the gate and a second parasitic capacitor is formed between the second side of the drain and the gate, wherein the second parasitic capacitor comprises the second side of the drain and a compensation structure extending from the gate or the gate line; and

a pixel electrode disposed on a part of the drain and electrically connected to the drain through a via, so that a portion of the pixel electrode is substantially located between the gate and the compensation structure and substantially spaced apart from at least one of the gate and the compensation structure.

(*Emphasis Added*).

Claim 11 recites:

> 11. A liquid crystal display device with a capacitance-compensated structure, comprising:
> a first process layer comprising a gate line, a gate, and a compensation structure, wherein the gate is electrically connected to the gate line and the compensation structure connects to the gate; and
> a second process layer comprising a data line, a source, and a drain, wherein the source and the drain are formed corresponding to both sides of the gate, respectively, the source is electrically connected to the data line, the data line is substantially perpendicular to the gate line, the drain has a first side overlapping a portion of the gate and a second side overlapping a portion of the compensation structure; and
> ***a pixel electrode disposed on a part of the drain and electrically connected to the drain through a via, so that a portion of the pixel electrode is substantially located between the gate and the compensation structure and substantially spaced apart from at least one of the gate and the compensation structure;***
> wherein there is an acceptable alignment shift range between the first process layer and the second process layer, the sum of the capacitance of a first parasitic capacitor between the first side of the drain and the gate and a second parasitic capacitor between the second side of the drain and the compensation structure maintain a substantially constant value within the acceptable alignment shift range.

(*Emphasis Added*). Claims 1, 5, and 11 patently define over the cited art for at least the reason that the cited art fails to disclose or suggest the features emphasized above.

According to MPEP 2143, to establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. As set forth above, Applicant respectfully asserts that neither Ukita nor Moon teaches or reasonably suggests at least the features/limitations that have been emphasized above in independent claims 1, 5, and 11. As set forth above, Applicant

respectfully asserts that the rejection of claims 1, 5 and 11 is deficient and that these claims are in condition for allowance. Further, all remaining claims incorporate the limitations of either independent claim 1, 5, or 11, these remaining claims also are in condition for allowance.

No fee is believed to be due in connection with this submission. If, however, any additional fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully Submitted,

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